What is claimed:

1. A method for generating a graphical representation of a processing web of an instrument, comprising the steps of:

determining a first processing element of said processing web;

placing said first processing element in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

determining a second processing element of said processing web;

placing said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

connecting at least one pin of said first processing element to one pin of said second processing element.

2. The method of claim 1, wherein said connecting step connects an output pin of said first element to an input pin of said second element.

3. The method of claim 2, wherein said connecting step generates a line in said graphical representation between said output pin of said first element to said output pin of said second element.

4. The method of claim 3, wherein said line is drawn including one of a plurality of designations based upon a type of data being carried thereon.

5. The method of claim 4, wherein said plurality of designations are colors.

6. The method of claim 1 wherein said at least one pin of said first processing element and said at least one pin of said second processing element are coded based upon a type of data to output therefrom, or received thereby, respectively.

7. The method of claim 6, wherein said coding is by color.

8. The method of claim 6, wherein said coding is by symbol.

9. The method of claim 6, wherein said coding is by graphical designation.

10. The method of claim 1, wherein said first processing element is updated at a faster rate and said second processing element is updated at a slower rate.

11. The method of claim 10, wherein said update said first processing element and update of said second processing element are synchronized.

12. The method of claim 10, wherein said update of said first and second processors is controlled by an update processing element.

13. The method of claim 1, wherein a viewing object may be placed at any location on the graphical representation to see a current, live output at that location.

14. A method for generating a graphical representation of a processing web of an instrument, comprising the steps of:

determining a first processing element of said processing web;

placing said first processing element in a particular location based at least in part upon its function and various inputs to and outputs from said first processing element;

determining a second processing element of said processing web;

placing said second processing element in a particular location based at least in part upon its function, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

connecting said first processing element to second processing element indicating a flow of data therebetween;

wherein said first processing element is a waveform acquisition processing; and

wherein said second processing element is a display processing element.

15. The method of claim 14, further comprising the steps of:

determining a third processing element of said processing web; and

placing said third processing element in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements.

wherein said third processing element performs an intermediate processing step between said first processing element and said second processing element.

16. The method of claim 14, further comprising the steps of:

determining a third processing element of said processing web;

placing said third processing element in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a static memory input.

17. The method of claim 14, further comprising the steps of:

determining a third processing element of said processing web;

placing said third processing element in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing

element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a display trace output including at least one processing function.

18. The method of claim 14, further comprising the steps of:

determining a third processing element of said processing web;

placing said third processing element in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a parameter output.

19. The method of claim 14, wherein said connection between said first processing element and said second processing element is provided in a color indicative of the type of data flowing therebetween.

20. The method of claim 14, wherein each of said first and second processing elements includes an indication of the number of inputs and outputs thereof.

21. The method of claim 14, wherein said inputs and outputs are provided in a color indicative of the type of data to be received or output thereon.

22. A method for modifying a processing sequence by editing the configuration of a processing web, comprising the steps of:

determining a current state of said processing web; and

editing at least one processing element of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one processing element.

23. The method of claim 22, further comprising the step of updating said first processing element indicating a time during which said first processing element is to consume additional input data.

24. The method of claim 23, wherein said update is controlled by an update processing element.

25. The method of claim 22, wherein said editing of said at least one processing element includes changing a connection of at least one pin of said at least on processing element.

26. The method of claim 22, wherein said editing of said at least one processing element includes adding another processing element to said processing web.

27. The method of claim 26, wherein said another processing element is added to said processing web by dragging a representation of said processing element onto a display representative of said processing web, and connecting inputs and outputs of said another processing element to the inputs and outputs of other existing processing elements.

28. The method of claim 22, wherein said editing of said at least one processing element includes modifying the definition thereof.

29. The method of claim 28, wherein modifying the definition of said at least one processing element includes modifying one or more operating parameters thereof.

30. The method of claim 22, further comprising the step of adding a viewing element to said graphical representation of said processing web to view a live, real time output at the location of said viewing element.

31. A method for modifying a processing sequence by editing the graphical representation of a processing web as displayed on a processing web editor, comprising the steps of:

determining a current state of said processing web;

generating a graphical representation of said processing web by:

determining a first processing element of said processing web;

placing said first processing element in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

determining a second processing element of said processing web;

placing said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

connecting at least one pin of said first processing element to one pin of said second processing element; and

editing at least one processing element of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one processing element.

32. A graphical representation of a processing web of an instrument, comprising:

a first processing element of said processing web, said first processing element being placed in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

a second processing element of said processing web, said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

a connection for connecting at least one pin of said first processing element to one pin of said second processing element.

33. The graphical representation of the processing web of claim 32, wherein said connection connects an output pin of said first element to an input pin of said second element.

34. The graphical representation of the processing web of claim 33, wherein said connection generates a line in said graphical representation between said output pin of said first element to said output pin of said second element.

35. The graphical representation of the processing web of claim 33, wherein said line is drawn including one of a plurality of designations based upon a type of data being carried thereon.

36. The graphical representation of the processing web of claim 35, wherein said plurality of designations are colors.

37. The graphical representation of the processing web of claim 32, wherein said at least one pin of said first processing element and said at least one pin of said second processing element are coded based upon a type of data to output therefrom, or received thereby, respectively.

38. The graphical representation of the processing web of claim 37, wherein said coding is by color.

39. The graphical representation of the processing web of claim 37, wherein said coding is by symbol.

40. The graphical representation of the processing web of claim 37, wherein said coding is by graphical designation.

41. The graphical representation of the processing web of claim 32, wherein said first processing element is updated at a faster rate and said second processing element is updated at a slower rate.

42. The graphical representation of the processing web of claim 41, wherein said update said first processing element and update of said second processing element are synchronized.

43. The graphical representation of the processing web of claim 41, wherein said update of said first and second processors is controlled by an update processing element.

44. The graphical representation of the processing web of claim 32, wherein a viewing object may be placed at any location on the graphical representation to see a current, live output at that location.

45. A graphical representation of a processing web of an instrument, comprising:

a first processing element of said processing web, said first processing element being placed in a particular location based at least in part upon its function and various inputs to and outputs from said first processing element;

a second processing element of said processing web, said second processing element in a particular location based at least in part upon its function, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

a connection for connecting said first processing element to second processing element indicating a flow of data therebetween;

wherein said first processing element is a waveform acquisition processing element; and

wherein said second processing element is a display processing.

46. The graphical representation of the processing web of claim 45, further comprising:

a third processing element of said processing web, said third processing element being placed in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements.

wherein said third processing element performs an intermediate processing step between said first processing element and said second processing element.

47. The graphical representation of the processing web of claim 45, further comprising:

a third processing element of said processing web, said third processing element being placed in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a static memory input.

48. The graphical representation of the processing web of claim 45, further comprising:

a third processing element of said processing web, said third processing element being placed in a particular location based at least in part upon its function in said processing web,

various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a display trace output including at least one processing function.

49. The graphical representation of the processing web of claim 45, further comprising:

a third processing element of said processing web, said third processing element being placed in a particular location based at least in part upon its function in said processing web, various inputs to and outputs from said second processing element, and a relationship between said third processing element and said first and second processing elements;

wherein said third processing element is a parameter output.

50. The graphical representation of the processing web of claim 45, wherein said connection between said first processing element and said second processing element is provided in a color indicative of the type of data flowing therebetween.

51. The graphical representation of the processing web of claim 45, wherein each of said first and second processing elements includes an indication of the number of inputs and outputs thereof.

52. The graphical representation of the processing web of claim 51, wherein said inputs and outputs are provided in a color indicative of the type of data to be received or output thereon.

53. An editor for modifying a processing sequence by editing the configuration of a processing web, comprising:

means for determining a current state of said processing web, including one or more processing elements and connections therebetween in said processing web; and

a selector for selecting and editing at least one of said processing elements of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one processing element.

54. The editor of claim 53, wherein said editor edits said first processing element to indicate an update time indicating a time during which said first processing element is to consume additional input data.

55. The editor of claim 54, wherein said update is controlled by an update processing element.

56. The editor of claim 53, wherein said editing of said at least one processing element includes changing a connection of at least one pin of said at least on processing element.

57. The editor of claim 53, wherein said editing of said at least one processing element includes adding another processing element to said processing web.

58. The editor of claim 57, wherein said another processing element is added to said processing web by dragging a representation of said processing element onto a display representative of said processing web, and connecting inputs and outputs of said another processing element to the inputs and outputs of other existing processing elements.

59. The editor of claim 53, wherein said editing of said at least one processing element includes modifying the definition thereof.

60. The editor of claim 59, wherein modifying the definition of said at least one processing element includes modifying one or more operating parameters thereof.

61. The editor of claim 53, further comprising a viewing element being added to said processing web to view a live, real time output at the location of said viewing element.

62. A processing web editor for modifying a processing sequence by editing a graphical representation of a processing, comprising:

means for determining a current state of said processing web;

a renderer for generating a graphical representation of said processing web by:

determining a first processing element of said processing web;

placing said first processing element in a particular location based at least in part upon its location in said processing web and various inputs to and outputs from said first processing element;

determining a second processing element of said processing web;

placing said second processing element in a particular location based at least in part upon its location in said processing web, various inputs to and outputs from said second processing element, and a relationship between said second processing element and said first processing element; and

connecting at least one pin of said first processing element to one pin of said second processing element; and

a selector for selecting and editing at least one processing element of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one processing element.

63. The editor of claim 62, wherein a list of available processing elements is provided.

64. The editor of claim 63, wherein these processing elements are categorized by function.

65. The editor of claim 62, wherein upon selection of a processing element allows for the modifying of any parameter regarding said selected processing element

66. An editor for modifying a processing sequence by editing the configuration of a processing web, comprising:

means for determining a current state of said processing web, including one or more processing elements and connections therebetween in said processing web; and

a selector for selecting and editing at least one connection between said processing elements of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one connection.

67. The editor of claim 66, wherein when said at least one connection is requested to be edited, a determination is made whether said processing elements to be connected by said at least one connection are compatible.

68. The editor of claim 67, wherein if it is determined that said processing elements are compatible and of the same format, the connection is made.

69. The editor of claim 67, wherein if it is determined that said processing elements are compatible but of different formats, an adapter is automatically inserted between the processing elements.

70. The editor of claim 69, wherein said adapter comprises a plurality of processing elements.

71. The editor of claim 67, wherein if it is determined that said processing elements are not compatible, a connection is not made therebetween.

72. An method for modifying a processing sequence by editing the configuration of a processing web, comprising the steps of:

determining a current state of said processing web, including one or more processing elements and connections therebetween in said processing web; and

selecting and editing at least one connection between said processing elements of said processing web;

whereby said processing sequence is modified in accordance with the editing of said at least one connection.

73. The method of claim 72, wherein when said at least one connection is requested to be edited, determining whether said processing elements to be connected by said at least one connection are compatible.

74. The method of claim 73, wherein if it is determined that said processing elements are compatible and of the same format, the connection is made.

75. The method of claim 73, wherein if it is determined that said processing elements are compatible but of different formats, an adapter is automatically inserted between the processing elements.

76. The method of claim 75, wherein said adapter comprises a plurality of processing elements.

77. The method of claim 73, wherein if it is determined that said processing elements are not compatible, a connection is not made therebetween.